Abstract of the Disclosure

An operational margin of a memory of a semiconductor integrated circuit device including an SRAM is improved. In order to set the Vth of driving MISFETs Qd, transfer MISFETs Qt and MISFETs for load resistance QL forming memory cells of an SRAM, relatively and intentionally higher than the Vth of predetermined MISFETs of SRAM peripheral circuits and logic circuits such as microprocessor, an impurity introduction step is introduced to set the Vth of the driving MISFETs Qd, transfer MISFETs Qt and MISFETs for load resistance, separately from an impurity introduction step for setting the Vth of the predetermined MISFETs.